XPAC/WinPAC Interrupt Performance Test

Overview

For high-performance embedded applications (PAC, P**rogrammable Automation Controller),** the need for time-critical response and real-time performance is indispensable. A **Real-time Operating System** (RTOS) which is a computing environment that reacts to input within a specific time period, is needed for these applications on a PAC.

Applications where specific timings are requested include:

- Hard real time:
  Applications where system fails if timings are not met
- Soft real time:
  Applications where the system tolerates large timing latencies
- Actual timing requirements are system-specific

The following items are used to assess the Windows CE design in terms of the most common hard real-time requirements:

- Interrupt latency prediction and reduction
- Control of interrupt handling by the OEM
- Predictable system response
- Thread access to system interval timer
- Thread context and synchronization
- Thread priority support
- Thread switching
- Time slicing

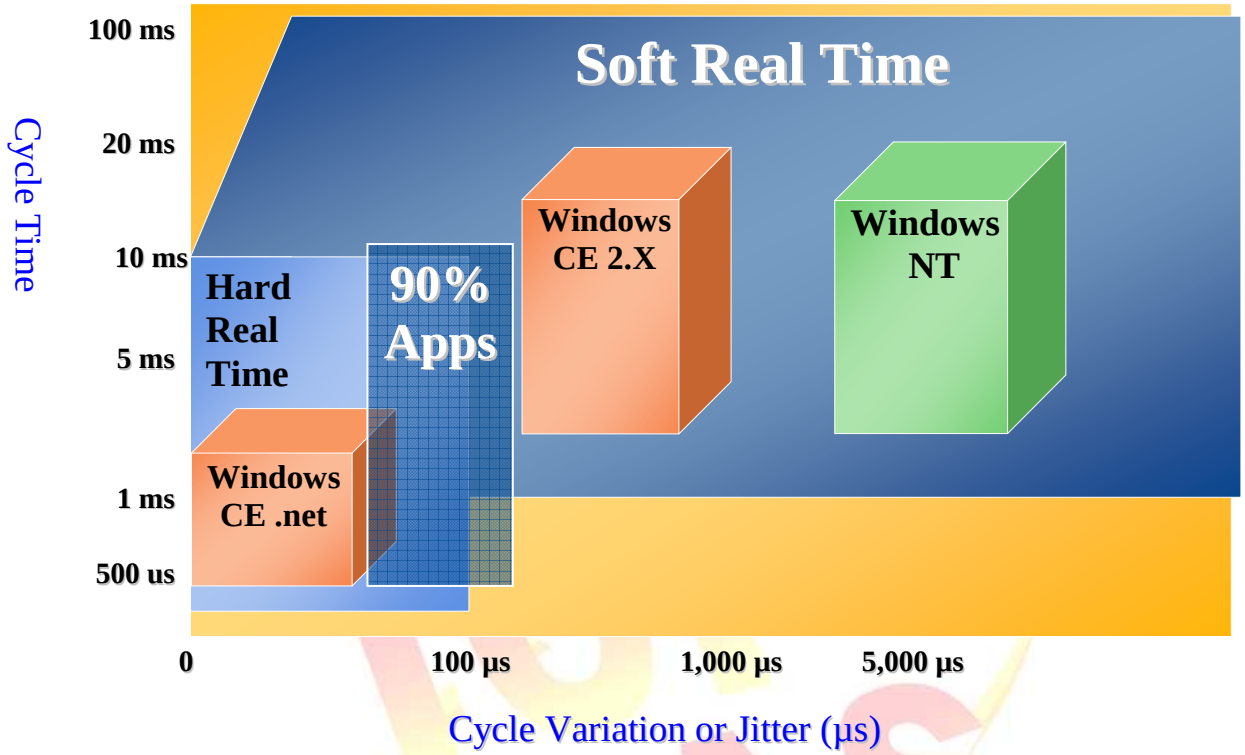
Microsoft Windows CE.NET is an operating system that incorporates **hard real-time capabilities** and is embedded in the WinPAC/XPAC series.

Reference:

- **http://www.scribd.com/doc/18269801/Wince-Realtime**
- **http://msdn.microsoft.com/en-us/library/ms836770.aspx**

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OMAC represents Industrial Automation Community



Note:

The Open Modular Architecture Control Users' Group (**OMAC**, Research Triangle Park, NC) has changed its name to the Organization for Manufacturing Automation and Control (OMAC) to reflect an evolution of the group's mission.

http://findarticles.com/p/articles/mi_qa3618/is_200810/ai_n30992784/?tag=rel.res3

http://www.omac.org/

Basic Terminology

Interrupt

An interrupt is a Hardware signal indicates that a real-world event has occurred

The corresponding hardware device needs to be serviced by the computer system in some way.

Latency

Latency describes the time from when the interrupt occurred to when the hardware begins to be serviced.

Jitter

Jitter defines the range of allowable variations in service times, and is usually defined by the “tolerance” of a mechanical system for variability in the response.

Bounded

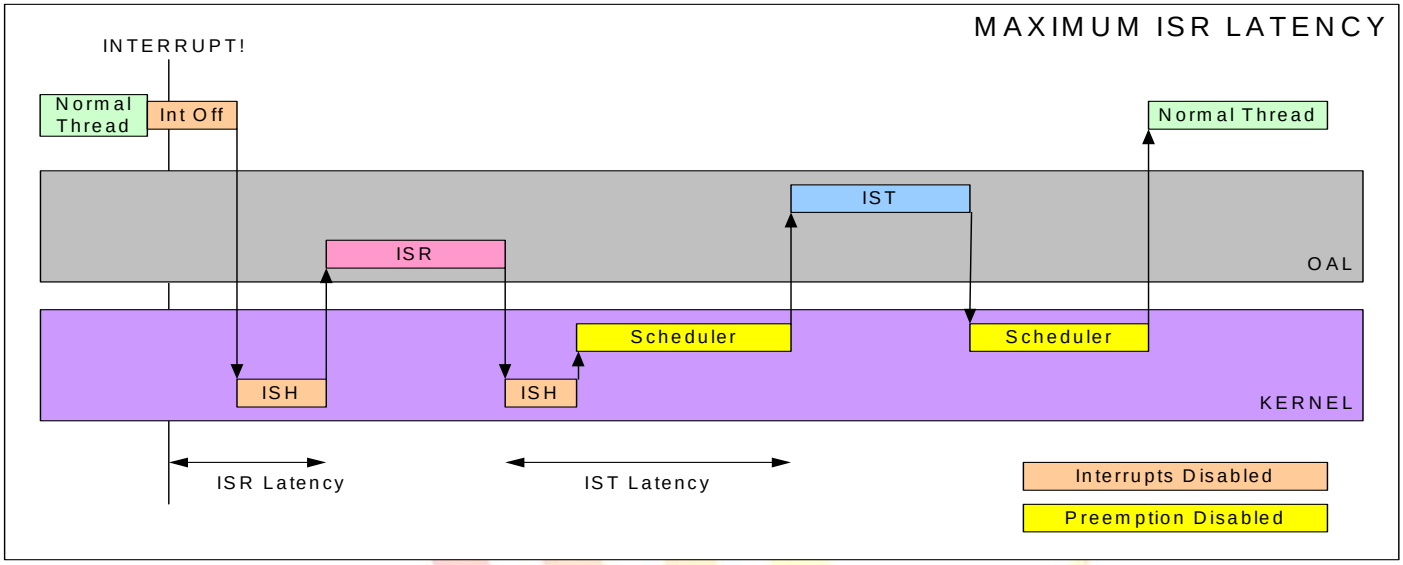
Bounded indicates the extreme limits that are known precisely.

The combination of bounded low latency and jitter = “hard” real time

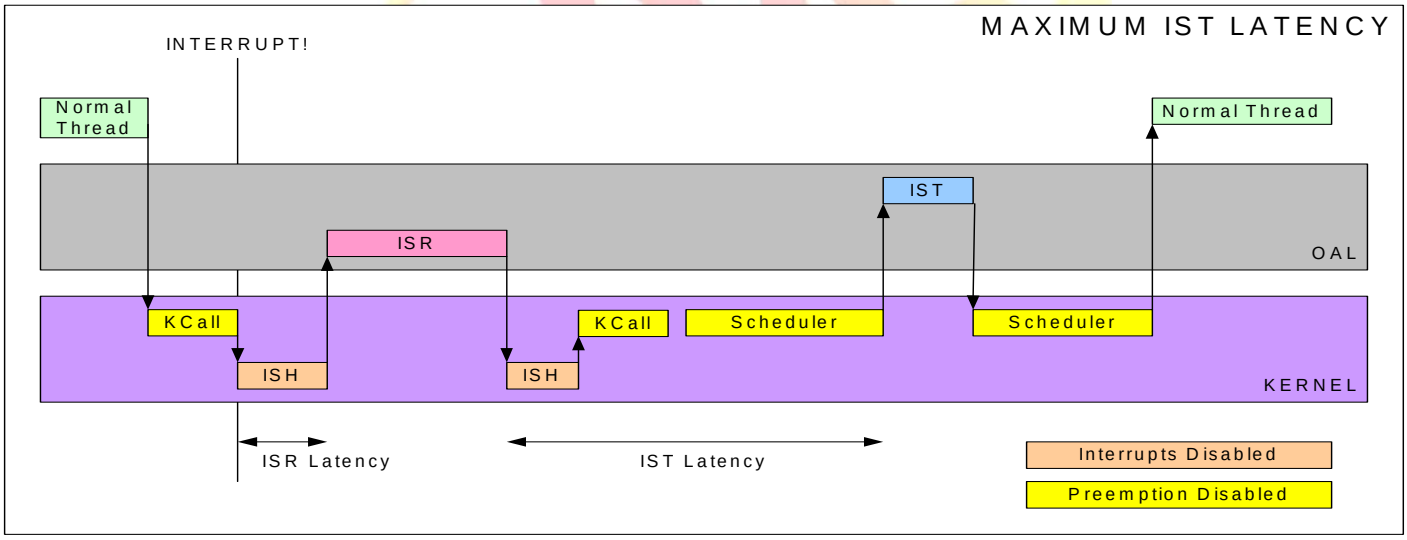
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ISR/IST Latency definition

Maximum ISR Latency Path



Maximum IST Latency Path



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Interrupt Measurement Tools

ILTiming.exe is a testing tool that allows an OEM to measure an interrupt service routine (ISR) and the interrupt service thread (IST) latency

Iltiming.exe Test for ICPDAS's PAC

Comparison (Units: microseconds µs)

	Min.		Avg.		Max.	
ISR/IST	ISR Latency	IST Latency	ISR Latency	IST Latency	ISR Latency	IST Latency
XPAC8000_CE6_Atom	5.0	13.4	5.0	14.0	5.0	14.2
XPAC8000_CE6_LX800	5.8	12.5	6.7	14.1	7.5	15.0
WP8000/ViewPAC (PXA270)	4.9	24.3	5.1	25.5	6.4	31.3

Reference:

http://msdn.microsoft.com/en-us/library/ee483144%28WinEmbedded.60%29.aspx

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Benchmarking Real-time Determinism in PAC

IST/ISR Latency and Jitter Test

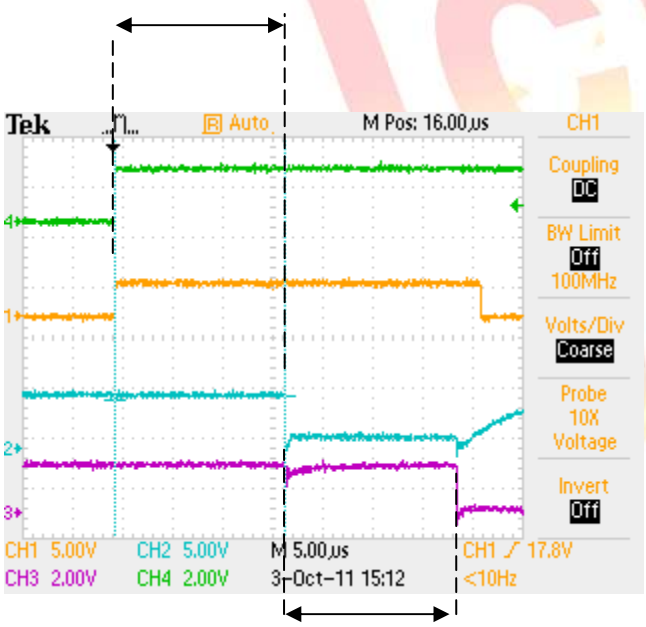
Test Equipment:

XP-8341-CE6 XP-8341-Atom-CE6 WP-8441
i-8048W * 1 (Digital Input with Interrupt Module)
i-8055W * 1 (Non-isolated Open-collector DO module)
Signal Generator: Agilent 33210A
Oscilloscope: Tektronix TDS2014B

Test method and procedure:

1. Install i-8048W DI module and i-8055W DO module on a PAC (XPAC/ WinPAC).
2. Use a signal generator to create a signal to channel 0 of i-8048W. This interrupt pulse signal was also connected to CH 1 (yellow line) of the oscilloscope for monitoring purposes.
3. The ISR[Note1] signal was connected to CH 2 (Blue line) and the IST[Note2] single was connected to CH3 (Pink line) of the oscilloscope.

ISR Latency



IST Latency

CH1 (Yellow Line): Interrupt trigger from i-8048W
CH2 (Blue Line): ISR time for i-8048W
CH3 (Pink Line): IST time for i-8048W

4. Send a signal to a controller and measure how long it takes to respond. The "latency time" and the "jitter time" for this response are the quantified measures of determinism.

Note1 The ISR signal is generated by DO0 channel of i-8055W, and is generated from the ISR code of the OS kernel when i-8044W channel receives the external trigger signal.

Note2 The IST signal is generated by DO1 channel of i-8055W, and is generated by the thread code of this application when the kernel (ISR) passes the signal to the interrupt thread (IST).

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5. Continually send a square wave input to channel 0 of i-8048W at a frequency of 5KHz (a 200 microsecond pulses period) using a pulse generator set at a duty cycle of 50 percent.
6. Set the system loading to 100% and use the persistence feature of the oscilloscope. This feature records and overwrites ALL traces for a total of many hundreds of thousands of traces for 24 hours.
7. The results of the ISR/IST latency and the Jitter time can be measured from the oscilloscope.

Results:

Comparison (Units: microsecond μs)

	Avg. (Min. /Max.)		
ISR/IST	**ISR Latency**	**IST Latency**	**Jitter**
XPAC8000_CE6_Atom	22 (21/28)	15 (13.8/24.4)	10
XPAC8000_CE6_LX800	17 (16/23.2)	17.2 (18/24)	10
WP8000 (PXA270)	19.6 (14 / 21)	51.6 (44/ 122)	100

Note:

Thread Priority set to 100

References:

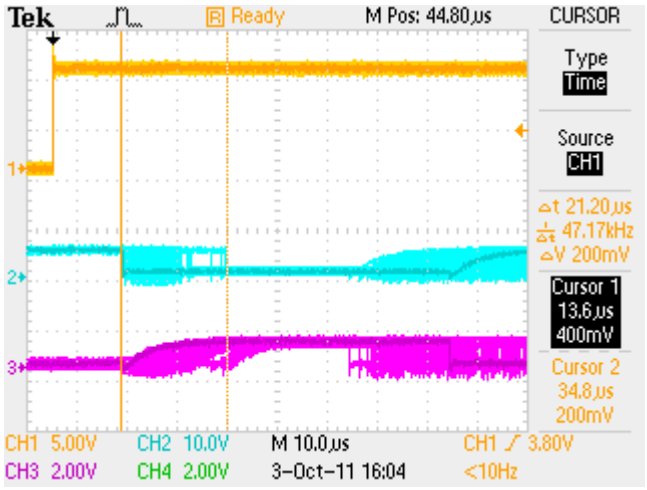
http://msdn.microsoft.com/en-us/library/ms836535.aspx for Benchmarking Real-time Determinism in Microsoft Windows CE

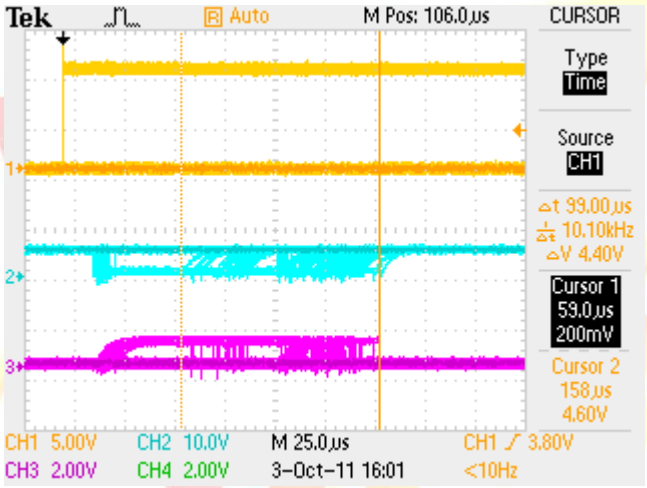
http://www.icpdas.com/products/Remote_IO/i-8ke/i-8048w.htm for more details regarding to i-8048W

http://www.icpdas.com/products/Remote_IO/i-8ke/i-8055w.htm for i-8055W

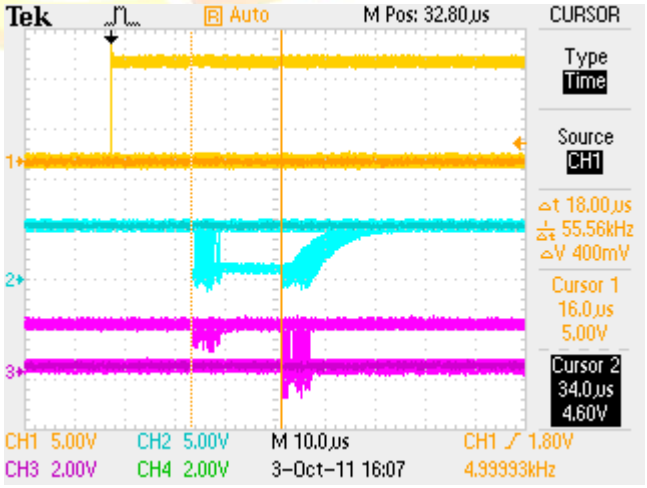
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PXA270

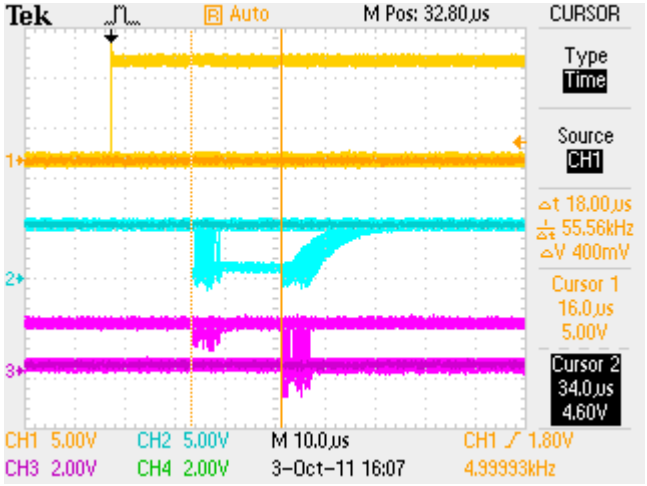




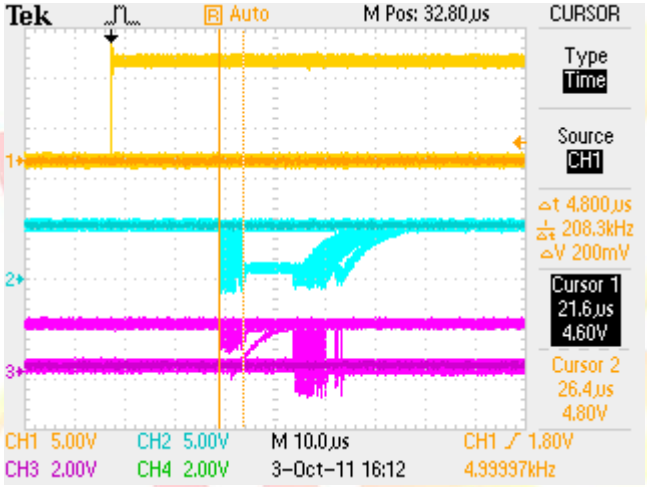
LX800

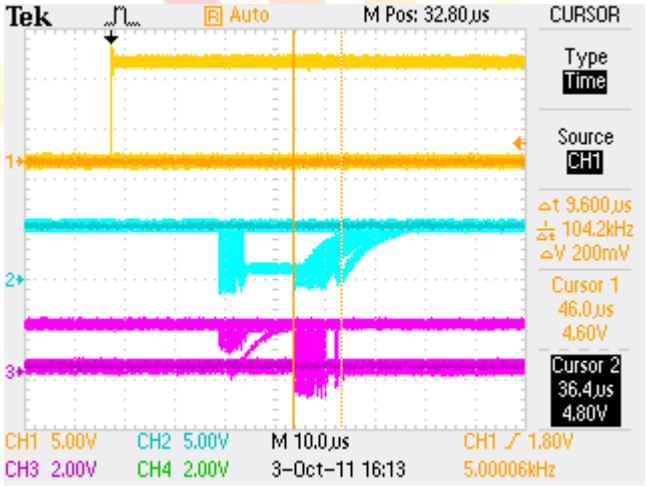


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Atom





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