XV161-SL User Manual

XV I/O Board for Stack Light Monitor

Mar. 2026, Version 1.01



Warranty

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1. Introduction

XV161-SL is a stack light monitoring XV I/O expansion board. It includes with 6 channels of DC digital input and 1 channel of relay output. It can be used to monitor the status of the stack light of the MES (Manufacturing Execution System) machines.
The XV board can be used to detect the status of each color segment of the stack light as being either OFF, ON, or Flashing. In addition to detecting the status of each individual color segment, the status of the combination of multiple color segments can also be defined, including the ability to report the duration of the previous status.



WP-2241, LP-2241, UA-2241, WISE-2241, PMC-2241 Series



WP-5231/LP-5231/UA-5231, WISE-5231/PMC-5231 Series



VPD-132/133 Series VPD-142/143 Series

1.1 Features

- Able to detect the status of each color segment: ON, OFF, or Flashing
- 6 channel DC digital input and 1 channel alarm relay output
- Users-define multiple color segment combinations for status monitoring
- Reports the duration of the previous status
- Digital input provides 70 VDC overvoltage protection
- Digital output provides power-on value and safe value settings

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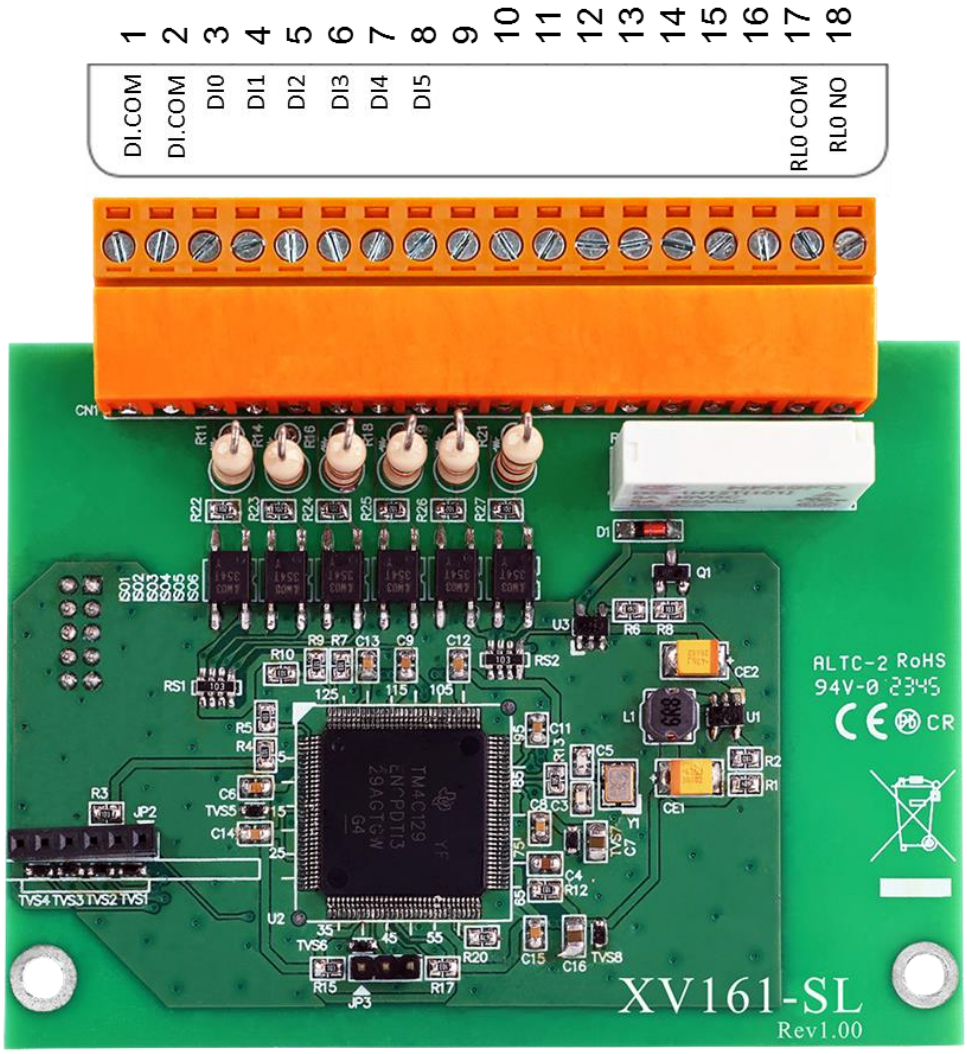
1.2 I/O Specification

Digital Input		
Channels		6
Input Type		Wet Contact (Sink / Source)
ON Voltage Level		+10 VDC ~ 50 VDC
OFF Voltage Level		+4 VDC Max.
Input Impedance		10 kΩ, 0.5 W
Max. Stack Light Flashing Speed		3 kHz
Detect light status		Can detect the ON, OFF or Flashing status of each color light
User-defined status combination monitoring		Max. 81 combinations
Previous Status Duration Report		10 ~ 65500 Sec.
Overvoltage protection		70 VDC
Isolation		3750 VDC
Digital Output		
Channels		1
Output Type		Power Relay, Form A (SPST N.O.)
Operating Voltage		250 VAC / 30 VDC
Max. Load Current		5 A
Operate Time		6 ms
Release Time		3 ms
Electrical Endurance (Resistive Load)	VDE	5 A @ 250 VAC 30,000 ops (10 ops/min) at 75℃
		5 A @ 30 VDC 70,000 ops (10 ops/min) at 75℃
	UL	5 A @ 250 VAC/30 VDC 6,000 ops
		3 A @ 250 VAC/30 VDC 100,000 ops
Mechanical Life		20,000,000 ops at no load (300 ops/minute)
Power-on Value		Yes, Programmable
Safe Value		Yes, Programmable

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1.3 Pin Assignment

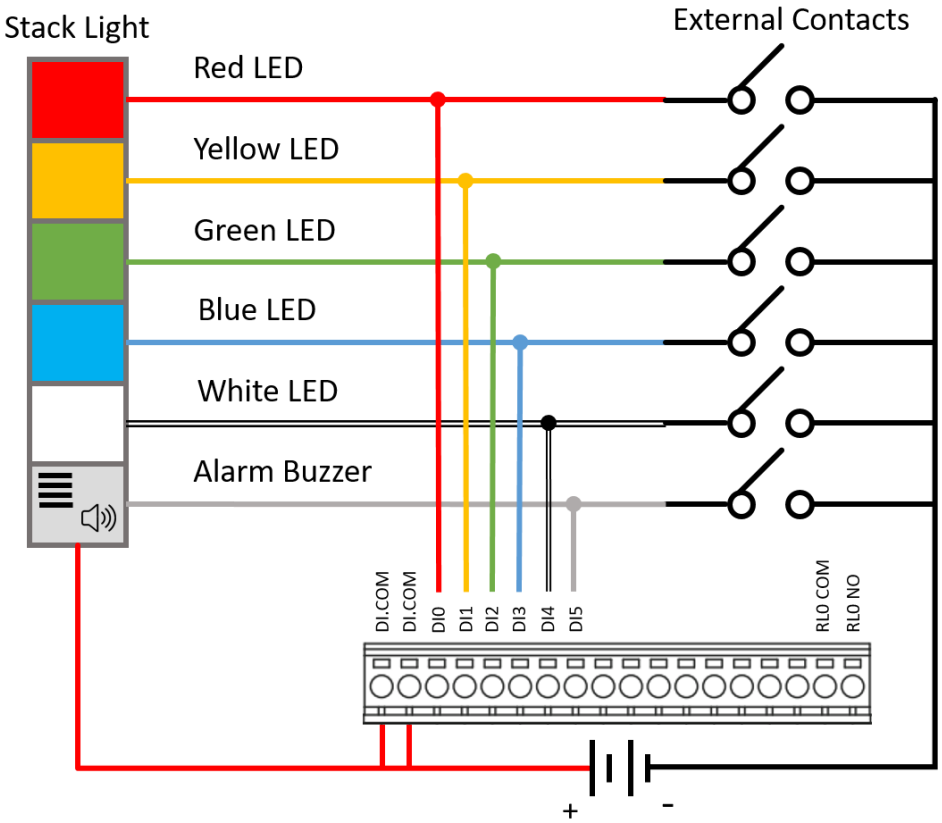


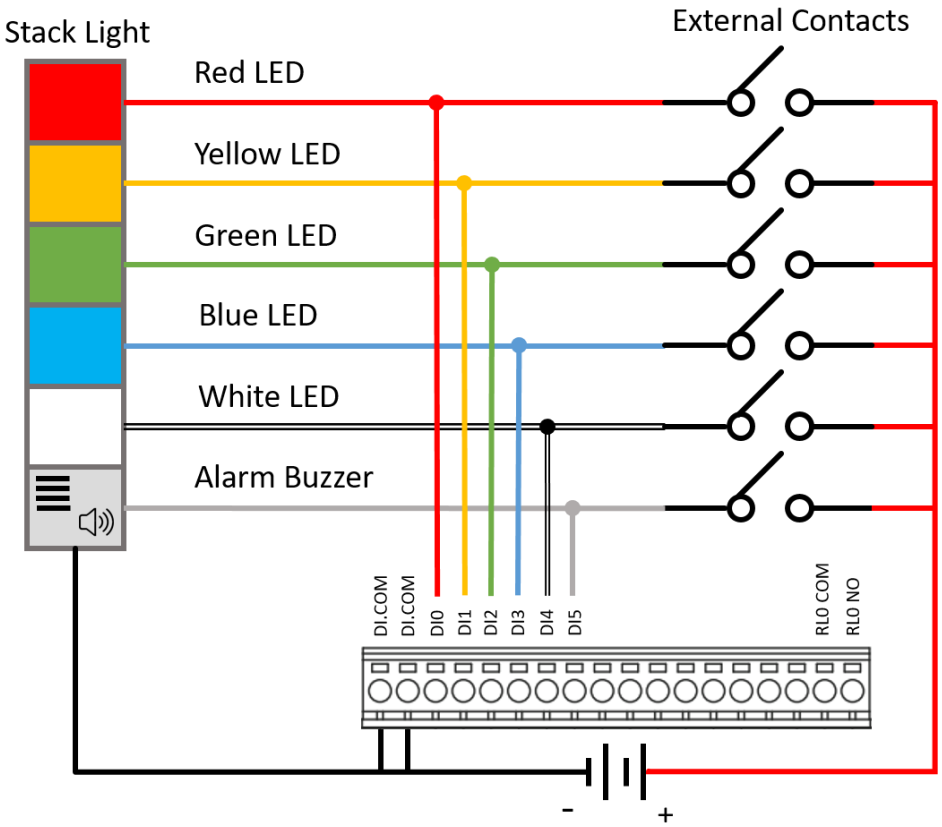
No.	Pin Name	Description
1	DI.COM	DI Common (Support Sink / Source Mode)
2	DI.COM	DI Common (Support Sink / Source Mode)
3	DI 0	Digital Input Pin 0
4	DI 1	Digital Input Pin 1
5	DI 2	Digital Input Pin 2
6	DI 3	Digital Input Pin 3
7	DI 4	Digital Input Pin 4
8	DI 5	Digital Input Pin 5
9 ~ 16	N / A	Reserved
17	RL0 COM	Relay Output Common
18	RL0 NO	Relay Normally Open

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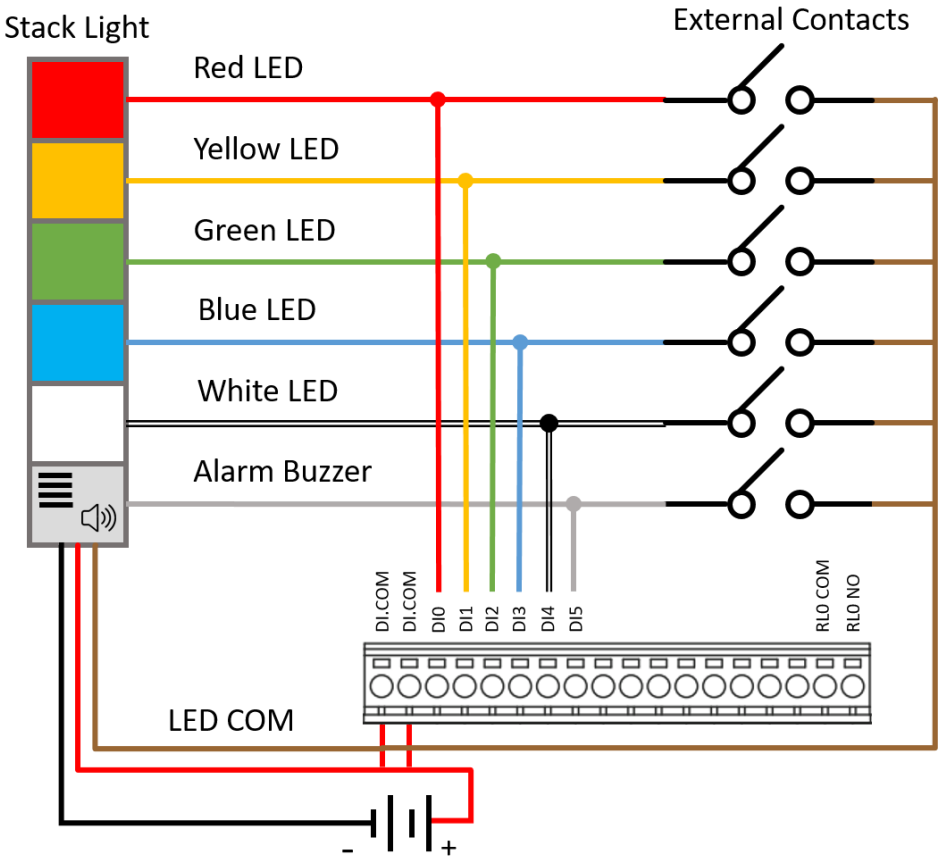
1.4 DI Wiring Connections



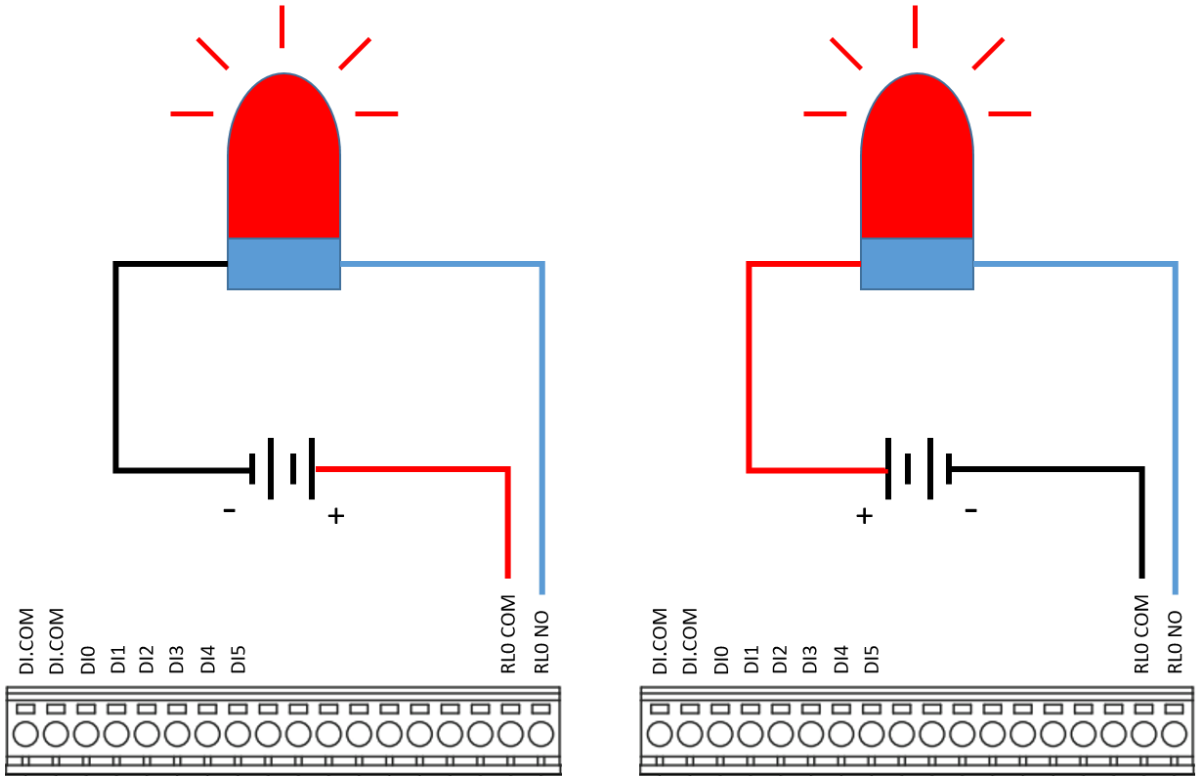


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1.5 Relay Wiring Connections



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2. Modbus Address Table

Coils: 0xxxx (Base 0) R: Read, W: Write, F: This setting will be saved in Flash

Starting Address		Points	Description	Data Format	Attribute
DEC	HEX				
0	0x00	1	Digital output channel	0: Off 1: On	R/W
160	0xA0	1	Sets the power-on value for DO channel	0: Off 1: On	R/W/F
192	0xC0	1	Sets the safe value for DO channel	0: Off 1: On	R/W/F
259	0x103	1	Host watchdog mode	0: Clear WDT flag mode 1: DO / AO mode	R/W/F
260	0x104	1	Host watchdog enable	0: Disable 1: Enable	R/W/F
269	0x10D	1	Host watchdog timeout status. Write 1 to clear the WDT flag.	0: Normal 1: Host watchdog timeout	R/W
Notes	Frequent writing to the Flash can cause it to become corrupt.				

Host watchdog mode (259 / 0x103):

0: Clear WDT flag mode: When this mode is selected, the host needs to periodically write 1 to Coil address 269 (0x10D) to clear the WDT flag to avoid a watchdog timeout.

1: DO / AO mode: When this mode is selected, the host needs to output DO or AO values regularly to avoid watchdog timeout.

Refer to Appendix A for the WDT Usage Flowchart.

Discrete Input: 1xxxx (Base 0) R: Read, W: Write, F: This setting will be saved in Flash

Starting Address		Points	Description	Data Format	Attribute
DEC	HEX				
16	0x10	1	Digital input channel	0: Off 1: On	R
256	0x100	1	1 to indicate Modbus RTU protocol	1: Modbus RTU	R
272	0x110	1	Reset status	0: not the initial read 1: Initial read	R

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Input Register: 3xxxx (Base 0) R: Read, W: Write, F: This setting will be saved in Flash

Starting Address		Points	Description	Data Format	Attribute
DEC	HEX				
0	0x0	6	Status of the monitored stack light	0: Off 1: On 2: Flashing	R
6 *	0x6	1	Current combinational status of the monitored stack lights	0 ~ 65535	R
7 *	0x7	1	Previous combinational status of the monitored stack lights	0 ~ 65535	R
8	0x8	1	Low word of the time of the Current combinational status of the monitored stack lights	0 ~ 65535 (sec)	R
9	0x9	1	High word of the time of the Current combinational status of the monitored stack lights	0 ~ 65535 (sec)	R
10	0xA	1	Low word of the time of the Previous combinational status of the monitored stack lights	0 ~ 65535 (sec)	R
11	0xB	1	High word of the time of the Previous combinational status of the monitored stack lights	0 ~ 65535 (sec)	R
100	0x64	1	Number of DI channels	6	R
110	0x6E	1	Number of DO channels	1	R
480	0x1E0	1	Low word of the Firmware Version	0x0000	R
481	0x1E1	1	High word of the Firmware Version	0x0100	R
482	0x1E2	1	Low word of the Module name	0x5601	R
483	0x1E3	1	High word of the Module name	0x6105	R

* About Current combinational status and Previous combinational status, please refer to **Stack light combinational status table (290 ~ 370 / 0x122 ~ 0x172)** of Holding Register**.**

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Holding Register: 4xxxx (Base 0) R: Read, W: Write, F: This setting will be saved in Flash

Starting Address		Points	Description	Data Format	Attribute
DEC	HEX				
201	0xC9	1	DI low-pass filter	0 ~ 10000 (ms) (default: 50)	R/W/F
288	0x120	1	DI status check interval	10 ~ 65530 (default: 50)	R/W/F
289	0x121	1	DI status evaluation count N	1 ~ 65530 (default: 50)	R/W/F
290	0x122	81	Stack light combinational status table	0 ~ 65535 (default: 0xFFFF)	R/W/F
484	0x1E4	1	Modbus ID Address 1 ~ 247	1 ~ 247	R/W/F
487	0x1E7	1	Modbus Response delay time	0 ~ 30 (ms)	R/W/F
488	0x1E8	1	Host watchdog timeout value	0 ~ 255 (0.1 sec)	R/W/F
491	0x1EB	1	Host watchdog timeout count	0 ~ 65535	R/W
Notes	Frequent writing to the Flash can cause it to become corrupt.				

DI low-pass filter (201 / 0xC9):

A low-pass Digital Input filter is a software function that can be used to eliminate high-frequency interference from input signals. The input state will only be changed when the width of any new signal is greater than the value specified as the filtering time, meaning that short, high-frequency interference pulses will be ignored. This is especially useful when attempting to eliminate contact bounce.

DI status check interval (288 / 0x120):

This parameter defines the time interval (in milliseconds) used to periodically check the On/Off status of each digital input (DI) channel.

For example, if set to 100 ms, the system will sample the DI input states every 100 ms. Any input state changes that occur between these sampling points will not be detected.

- The interval must be a multiple of 10 ms (e.g., 10, 20, 30…1000 ms).

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DI status evaluation count N (289 / 0x121):

This parameter defines the number of recent input status checks (based on the “DI status check interval”) that will be used to determine whether a digital input (DI) channel is **On**, **Off**, or **Flashing**.

- If no On/Off state change is detected in the most recent N/2 intervals, the DI state is considered **On** or **Off**, depending on the current input level.
- If 4 or more On/Off changes are detected within the most recent N intervals, the DI state is considered **Flashing**.

Stack light combinational status table (290 ~ 370 / 0x122 ~ 0x172):

Addresses 290 to 370 are defined as stack light combinational status entry 0 to 80. Each entry represents a combination of stack light status and is stored as a 16-bit word. Each 2-bit field encodes the status of one LED. Bit 0 and 1 encode DI 0, bit 2 and 3 encode DI 1 … bit 10 and 11 encode DI 5 and bits 12 to 15 are reserved. **When the value is 0xFFFF, it means that the address is disabled**. If the XV161-SL detected the corresponding combinational status, it will record the entry number of the combination at address 6 (**Current combinational status**) of “Input Register”.

For example, the status value of address 291 (entry 1) is 0x0123, the DI combinational status is as follows:

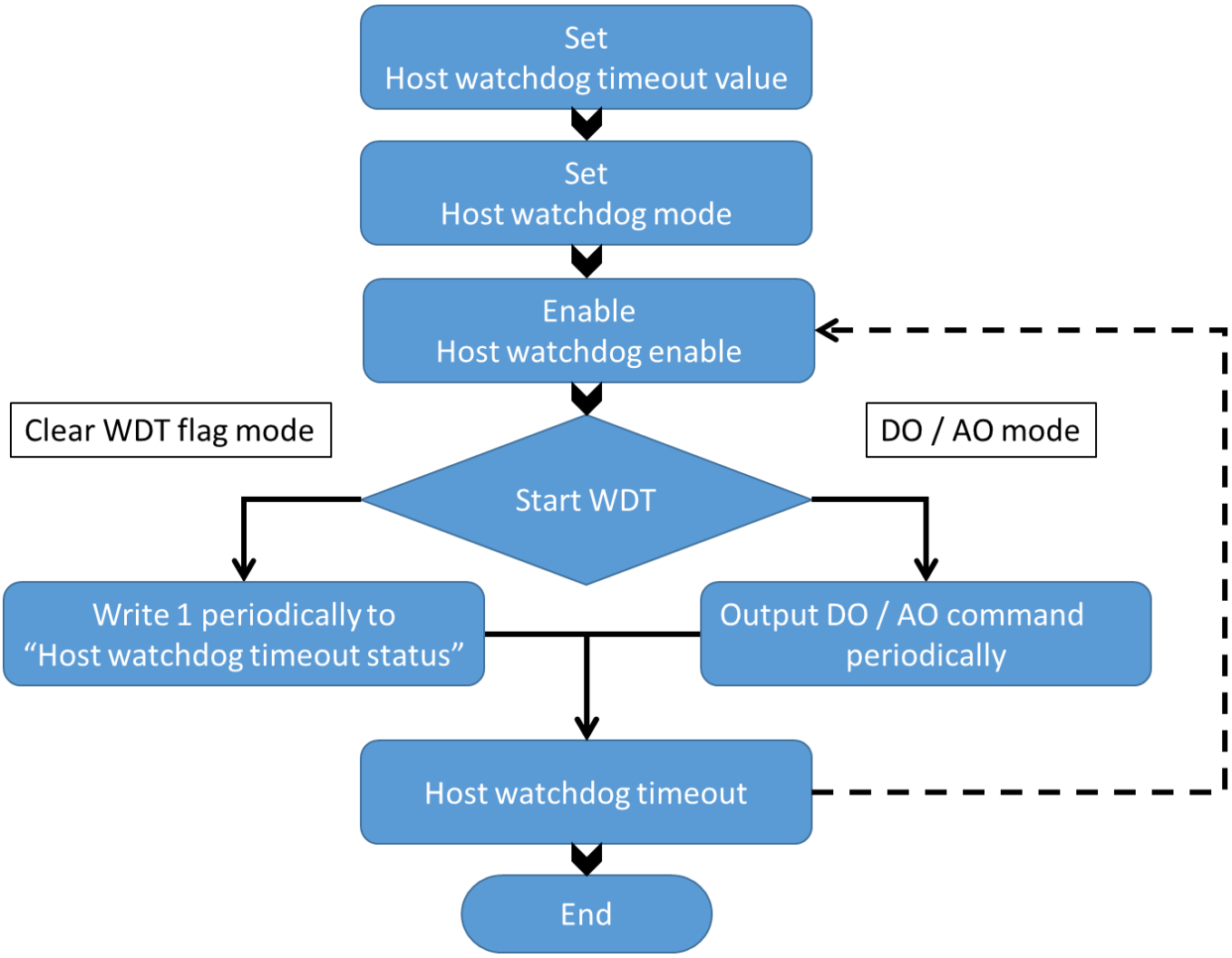
Hex	Binary		DI n	Status
3	Bit 1, 0	11	0	Don’t care
	Bit 3, 2	00	1	On
2	Bit 5, 4	10	2	Flashing
	Bit 7, 6	00	3	Off
1	Bit 9, 8	01	4	On
	Bit 11, 10	00	5	Off
0	Bit 13, 12	00	X	X
	Bit 15, 14	00	X	X

When the DIs match the above combination, entry number 1 will be recorded in the **“Current Combinational Status”** (Input Register address 0x6).

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Appendix A. WDT Usage Flowchart



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